03-18-02 HH 03 CD

Practition r's Docket No. RPS920000103US2 ***PATENT***

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Crockett et al;

Application No.: 10/054,542 Group No.: 2827

Filed: 01/22/2002 Examiner: unassigned

For: *INSERTION OF ELECTRICAL COMPONENT WITHIN A VIA OF A PRINTED CIRCUIT BOARD*

Assistant Commissioner for Patents
Washington, D.C. 20231

PETITION TO ESTABLISH PRIOR RECEIPT IN THE P.T.O. OF ITEMS CONSIDERED AS OMITTED BY THE P.T.O.--RESPONSE TO "NOTICE TO FILE CORRECTED APPLICATION PAPERS"

1. This is in response to the "NOTICE TO FILE CORRECTED APPLICATION PAPERS" mailed for this application on February 11, 2002. A copy of the "NOTICE TO FILE CORRECTED APPLICATION PAPERS" is enclosed.

CERTIFICATION UNDER 37 C.F.R. SECTION 1.10*

I hereby certify that this documents and the documents referred to as attached herein are being deposited with the United States Postal Service on this date March 15, 2002, in an envelope as "Express Mail Post Office to Addressee," mailing Label Number EL 888550280 US, addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231.

Amirah Scarborough
(type or print name of person mailing paper)

Amirah Scarborough
Signature of person mailing paper

EVIDENCE OF DEPOSIT OF ITEM(S) WITH APPLICATION INDICATED AS OMITTED IN THE "NOTICE TO FILE CORRECTED APPLICATION PAPERS"

2. In connection with the "Notice To File Corrected Application Papers" dated February 11, 2002, applicant submits the following evidence that the item(s) indicated as omitted were in fact deposited with the P.T.O. on January 22, 2002, which is the original date on which the papers for this application were deposited:

> The above stated patent application was filed as a divisional application of prior U.S. Application Serial No. 09/775250, the entire disclosure of the prior application, from which an oath or declaration was supplied under 37 CFR 1.63(d) should be considered as part of the disclosure of the divisional application filed on January 22, 2002 as incorporated by reference under 37 CFR 1.76 on the "Utility Patent Application Transmittal" and "Preliminary Amendment" filed on January 22, 2002. Applicant relies upon the incorporation for any portion of the application inadvertently omitted from the submitted application parts.

Nevertheless, applicant has supplied **Figure 4** of the divisional application and the **abstract** including a supplemental Declaration and Power of Attorney referring to the "omitted" items as requested on the Notice to File Corrected Application Papers dated Feb. 11, 2002.

3. In accordance with the requirements of the Notice of June 5, 1996, 61 Fed. Reg. 30,041-30,046, applicant hereby:

A. Petitions under 37 C.F.R. Section 1.53(e) for a review of the determination that the items in issue were omitted.

B. Submits the petition fee under 37 C.F.R. Section 1.17(i).

C. Submits evidence that the omitted items were in fact provided as described below.

4. Fee Payment

This is a **nonprovisional** application.

The petition fee, 37 C.F.R. Section 1.17(i), is paid as follows:

Charge Account No. 09-1990 the sum of $ 130.00.

A duplicate of this petition is attached.

Please charge Account No. 09-1990 for any fee deficiency for this petition.

5. Request for Refund

It is respectfully requested that, upon grant of the petition under 37 C.F.R. Section 1.53(e), the petition fee be refunded by deposit to Account No. 09-1990.

Date: 3/15/12

J Bruce Schelkopf
Registration No. 43901
919-543 4753
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INSERTION OF ELECTRICAL COMPONENT WITHIN A VIA OF A PRINTED CIRCUIT BOARD

A printed circuit board and method for reducing the impedance within the reference path and/or saving space within the printed circuit board. In one embodiment of the present invention, a printed circuit board comprises a plurality of conductive layers. The printed circuit board further comprises two or more vias for interconnecting two or more conductive layers. The printed circuit board further comprises an electrical component embedded in a particular via between two conductive layers to reduce the impedance within the reference path and/or save space within the printed circuit board.

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